REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 10-12-14	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, NONVOLATILE MEMORY, DUAL 1024-POSITION DIGITAL POTENTIOMETER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/11605**
	REV	**PAGE** 1 **OF** 12

AMSC N/A

5962-V015-11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance non volatile memory, dual 1024-position digital potentiometer microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer,s PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11605	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5235-EP	Nonvolatile memory, dual 1024-position digital potentiometer

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153	Small outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage referenced :
- V_{DD} to GND ..... -0.3 V to +7.0 V
- V_{SS} to GND ..... +0.3 V to -7.0 V
- V_{DD} to V_{SS} ..... 7.0 V
- V_A, V_B, V_W to GND ..... V_{SS} – 0.3 V to V_{DD} + 0.3 V

Current referenced, I_A, I_B, I_W:
- Pulsed 2/ ..... ±2.5 mA
- Continuous ..... ±1.1 mA

Digital input and output voltage to GND ..... -0.3 V to V_{DD} + 0.3 V
Ambient operating temperature range 3/ ..... -40°C to +125°C
Storage temperature range ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... 150°C
Lead temperature, soldering:
- Vapor phase (60 sec) ..... 215°C
- Infrared (15 sec) ..... 220°C

Thermal resistance, junction to ambient (θ_{JA}) ..... 150°C /W
Thermal resistance, junction to case (θ_{JC}) ..... 28°C /W
Package power dissipation ..... $(T_{J\,max} – T_A)/ \theta_{JA}$

2. APPLICABLE DOCUMENTS

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC STD 22	–	Electrically Erasable Programmable ROM (EEPROM) Program/Erase endurance and data retention test method A117
JEDEC STD 51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B and W terminals at a given resistance.
3/ Includes programming of nonvolatile memory.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing diagrams. The timing diagrams shall be as shown in figure 4 and 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
DC characteristic-RHEOSTAT mode (All RDACs)					
Resistor differential nonlinearity 4/	R-DNL		-2	+2	LSB
Resistor integral nonlinearity 4/	R-INL		-4	+4	LSB
Nominal resistor tolerance	$\Delta R_{AB}/R_{AB}$		-30	+30	%
Resistance temperature coefficient	$(\Delta R_{AB}/R_{AB})\Delta T \times 10^6$		35 TYP		ppm/°C
Wipe resistance	R_W	I_W = 1 V/R_{WB}, V_{DD} = 5 V, code = half scale		100	Ω
		I_W = 1 V/R_{WB}, V_{DD} = 3 V, code = half scale	200 TYP		
Nominal resistance match	R_{AB1}/R_{AB2}	Code = full scale, T_A = 25°C			%
DC characteristics – Potentiometer divider mode (All RDACs)					
Resolution	N			10	
Differential nonlinearity 5/	DNL		-2	+2	LSB
Integral nonlinearity 5/	INL		-4	+4	LSB
Voltage divider temperature coefficient	$(\Delta V_W/V_W)\Delta T \times 10^6$	Code = half scale	15 TYP		ppm/°C
Full scale error	V_{WFSE}	Code = full scale	-9	0	LSB
Zero scale error	V_{WZSE}	Code = zero scale	0	5	LSB
Resistor terminals					
Terminal voltage range 6/	V_A, V_B, V_W		V_{SS}	V_{DD}	V
Capacitance Ax, Bx 7/	C_A, C_B	f = 1 MHz, measured to GND, code = half scale	11 TYP		pF
Capacitance Wx 7/	C_W		80 TYP		
Common mode leakage current 7/ 8/	I_{CM}	$V_W = V_{DD}/2$		±2	µA
Digital inputs and outputs					
Input logic high	V_{IH}	With respect to GND, V_{DD} = 5 V	2.4		V
Input logic low	V_{IL}	With respect to GND, V_{DD} = 5 V		0.8	
Input logic high	V_{IH}	With respect to GND, V_{DD} = 3 V	2.1		
Input logic low	V_{IL}	With respect to GND, V_{DD} = 3 V		0.6	
Input logic high	V_{IH}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = -2.5 V	2.0		
Input logic low	V_{IL}	With respect to GND, V_{DD} = +2.5 V, V_{SS} = -2.5 V		0.5	
Output logic high (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V	4.9		
Output logic low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V		0.4	
Input current	I_{IL}			±2.25	µA
Input capacitance 7/	C_{IL}		5 TYP		pF
Power supplies					
Single supply power range	V_{DD}	V_{SS} = 0 V	3.0	5.5	V
Dual supply power range	V_{DD}/V_{SS}		±2.25	±2.25	V
Positive supply current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND		8	µA
Negative supply current	I_{SS}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = +2.5 V, V_{SS} = -2.5 V		7	µA
EEMEM store mode current	$I_{DD(store)}$	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$	35 TYP		mA
	$I_{SS(store)}$	V_{DD} = +2.5 V, V_{SS} = -2.5 V	-35 TYP		mA
EEMEM restore mode current 9/	$I_{DD(restore)}$	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = GND, $I_{SS} \approx 0$	0.3	9	mA
	$I_{SS(restore)}$	V_{DD} = +2.5 V, V_{SS} = -2.5 V	-0.3	-9	mA
Power dissipation 10/	P_{DISS}			50	µW
Power supply sensitivity 7/	P_{SS}			0.01	%/%

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Dynamic characteristics 7/ 11/					
Bandwidth	BW	-3 dB, V_{DD}/V_{SS} = ±2.5 V	125 TYP		kHz
Total harmonic distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz	0.05 TYP		%
V_W settling time	ts	$V_A = V_{DD}$, V_B = 0 V, V_W = 0.50% error band, Code 0x000 to code 0x200	4 TYP		µs
Resistor noise density	e_{N_WB}	T_A = 25°C	20 TYP		nV/√Hz
Crosstalk (C_{W1}/C_{W2})	C_T	$V_A = V_{DD}$, V_B = 0 V, measured V_{W1} with V_{W2} making full scale change	90 TYP		nV-s
Analog crosstalk	C_{TA}	$V_{DD} = V_{A1}$ = +2.5 V, $V_{SS} = V_{B1}$ = -2.5 V, measured V_{W1} with V_{W2} = 5 Vp-p@f = 1 kHz, Code 1 = 0x200, code 2 = 0x3FF	-81		dB
Interface timing and EEMEM reliability characteristics 12/					
Clock cycle time (t_{CYC})	t_1		20		ns
$\overline{CS}$ setup time	t_2		10		ns
CLK shut down time for $\overline{CS}$ rise	t_3		1		t_{CYC}
Input clock pulse width	t_4, t_5	Clock level high or low	10		ns
Data setup time	t_6	From positive CLK transition	5		
Data hold time	t_7	From positive CLK transition	5		
$\overline{CS}$ to SDO-SPI line acquire	t_8			40	
$\overline{CS}$ to SDO-SPI line release	t_9			50	
CLK to SDO propagation delay 13/	t_{10}	R_P = 2.2 kΩ, C_L < 20 pF		50	
CLK to SDO data hold time	t_{11}	R_P = 2.2 kΩ, C_L < 20 pF	0		
$\overline{CS}$ high pulse width 14/	t_{12}		10		
$\overline{CS}$ high to $\overline{CS}$ high 14/	t_{13}		4		t_{CYC}
RDY rise to $\overline{CS}$ fall	t_{14}		0		ns
$\overline{CS}$ rise to RDY fall time	t_{15}			0.3	ms
Store/Read EEMEM time 15/	t_{16}	Applies to instruction 0x2, 0x3, and 0x9	30 TYP		ms
$\overline{CS}$ rise to clock rise/Fall setup	t_{17}		15		ns
Preset pulse width (Asynchronous) 16/	t_{PRW}		50		ns
Preset response time to wiper setting 16/	t_{PRESP}	$\overline{PR}$ pulsed low to refresh wiper positions	140 TYP		µs
Power ON EEMEM restore time 16/	t_{EEMEM}		140 TYP		µs
Flash/EE memory reliability					
Endurance 17/			100		kCycles
Data retention 18/			100 TYP		Years

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 3 V to 5.5 V, V_{SS} =0; V_{DD} = 2.5 V, V_{SS} = -2.5 V, $V_A = V_{DD}$, $V_B = V_{SS}$, -40°C < T_A < 125°C (unless otherwise noted). The part can be operated at 2.7 V single supply, except from 0°C to -40°C, where a minimum of 3 V is needed.

3/ Typicals (TYP) represent average readings at 25°C and V_{DD} = 5V.

4/ Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. I_W ~ 50 µA for V_{DD} = 2.7 V and I_W ~ 400 µA for V_{DD} = 5 V.

5/ INL and DNL are measured at VW with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and $V_B = V_{SS}$. DNL specification limits of ±1 LSB maximum guaranteed monotonic operating conditions.

6/ Resistor terminal A, Resistor terminal B, and resistor terminal W has no limitations on polarity with respect to each other. Dual supply operation enables ground-referenced bipolar signal adjustment.

7/ Guaranteed by design and not subject to production test.

8/ Common mode leakage current is a measure of the dc leakage from any terminal A, terminal B, or terminal W to a common mode bias level of $V_{DD}/2$.

9/ EEMEM response mode current is not continuous. Current is consumed while EEMEM locations are read and transferred to the RDAC register. To minimize power dissipation, on a NOP, instruction 0 (0x0) should be issued immediately after instruction 1 (0x1).

10/ P_{DISS} is calculated from (I_{DD} x V_{DD}) + (I_{SS} x V_{SS}).

11/ All dynamic characteristics use V_{DD} = +2.5 V and V_{SS} = -2.5 V.

12/ Guaranteed by design and not subject to production test. See the timing diagrams section for the location of measured values. All input control voltages are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level 0f 1.5 V. Switching characteristics are measured using both V_{DD} = 3 V and V_{DD} = 5 V.

13/ Propagation delay depends on the value of V_{DD}, $R_{PULL-UP}$, and C_L.

14/ Valid for commands that do not activate the RDY pin.

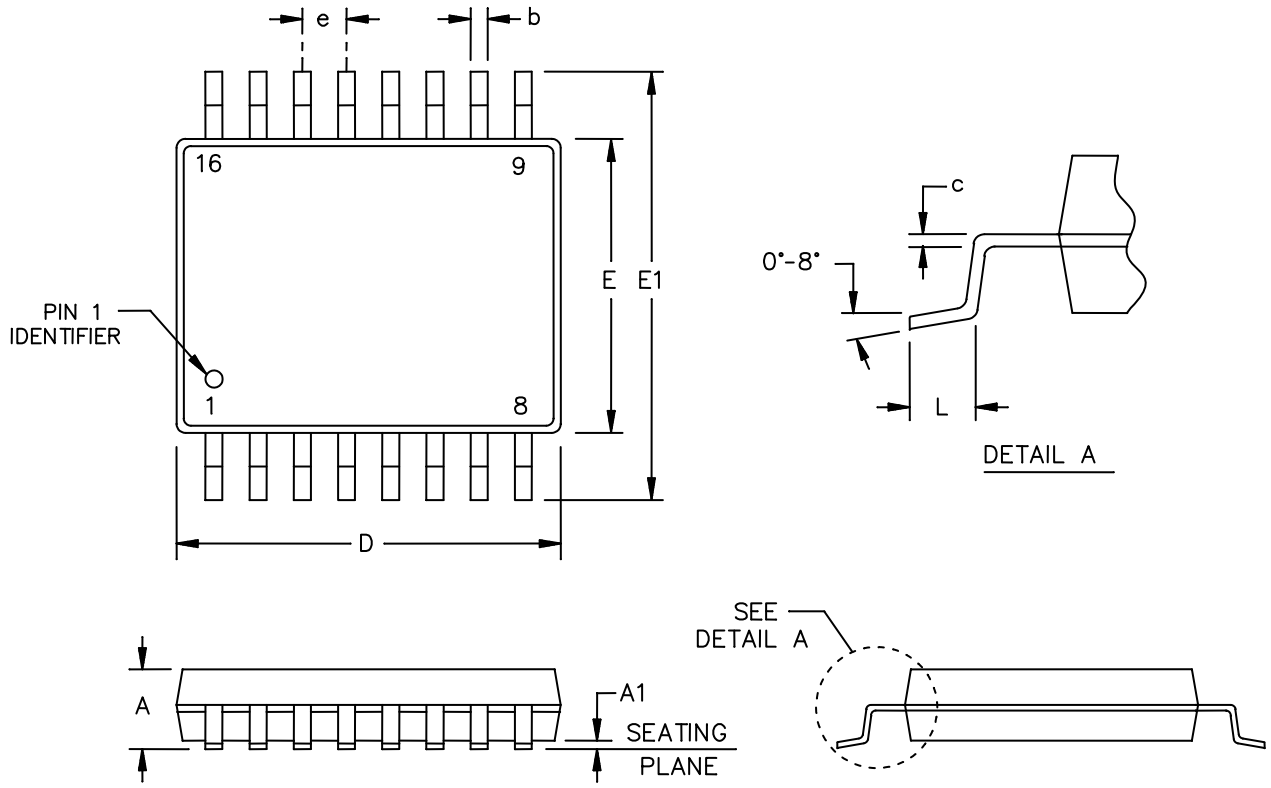
15/ RDY pin low only for Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and the $\overline{PR}$ hardware pulse; CMD_8 ~ 1; CMD_9, CMD_10 ~ 0.1 ms; CMD_2, CMD_3 ~ 20 ms. device operation at T_A = -40°C and V_{DD} < 3 V extends the save time to 35 ms.

16/ Not shown in FIGURE 4 and FIGURE 5.

17/ Endurance is qualified to 100,000 cycles per JEDEC standard 22, method A117 and measured at -40°C, +25°C, and +85°C; typical endurance at +25°C is 700,000 cycles.

18/ Retention life time equivalent at junction temperature (T_J) = 55°C per JEDEC standard 22, method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature in the Flash/EE memory.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 TYP	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

FIGURE 1. Case outline.

Case outline X

Pin No.	Mnemonic	Description
1	CLK	Serial Input Register Clock. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input. Shifts in one bit at a time on positive clock CLK edges. MSB loads first.
3	SDO	Serial Data Output. Serves readback and daisy-chain functions. Command 9 and Command 10 activate the SDO output for the readback function, delayed by 24 or 25 clock pulses, depending on the clock polarity before and after the data-word (see Figure 2 and Figure 3). In other commands, the SDO shifts out the previously loaded SDI bit pattern, delayed by 24 or 25 clock pulses depending on the clock polarity (see Figure 2 and Figure 3). This previously shifted out SDI can be used for daisy-chaining multiple devices. Whenever SDO is used, a pull-up resistor in the range of 1 kΩ to 10 kΩ is needed.
4	GND	Ground Pin, Logic Ground Reference.
5	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. If V_{SS} is used in dual supply, it must be able to sink 35 mA for 30 ms when storing data to EEMEM.
6	A1	Terminal A of RDAC1.
7	W1	Wiper terminal of RDAC1.ADDR(RDAC1)=0x0.
8	B1	Terminal B of RDAC1.
9	B2	Terminal B of RDAC2.
10	W2	Wiper terminal of RDAC2.ADDR(RDAC2)=0x1.
11	A2	Terminal A of RDAC2.
12	V_{DD}	Positive Power Supply.
13	$\overline{WP}$	Optional Write Protect. When active low, $\overline{WP}$ prevents any changes to the present contents, except $\overline{PR}$ strobe. CMD_1 and COMD_8 refresh the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high. Tie $\overline{WP}$ to V_{DD}, if not used.
14	$\overline{PR}$	Optional Hardware Override Preset. Refreshes the scratchpad register with current contents of the EEMEM register. Factory default loads midscale 512_{10} until EEMEM is loaded with a new value by the user. $\overline{PR}$ is activated at the logic high transition. Tie $\overline{PR}$ to V_{DD}, if not used.
15	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
16	RDY	Ready. Active high open-drain output. Identifies completion of Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and $\overline{PR}$.

FIGURE 2. Terminal connections.

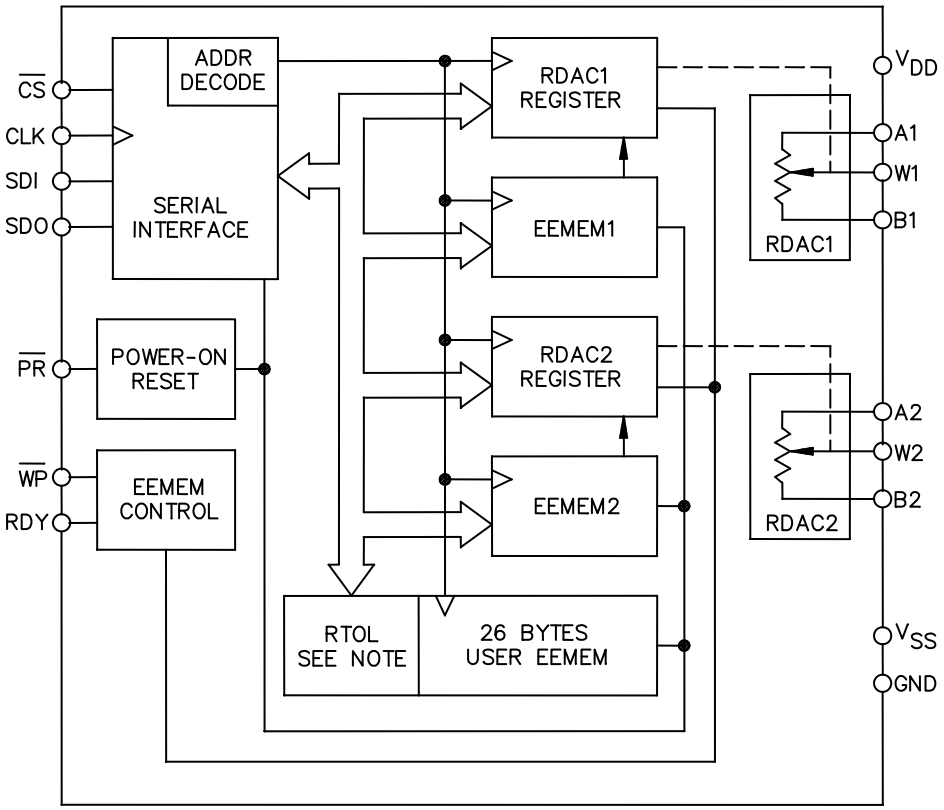
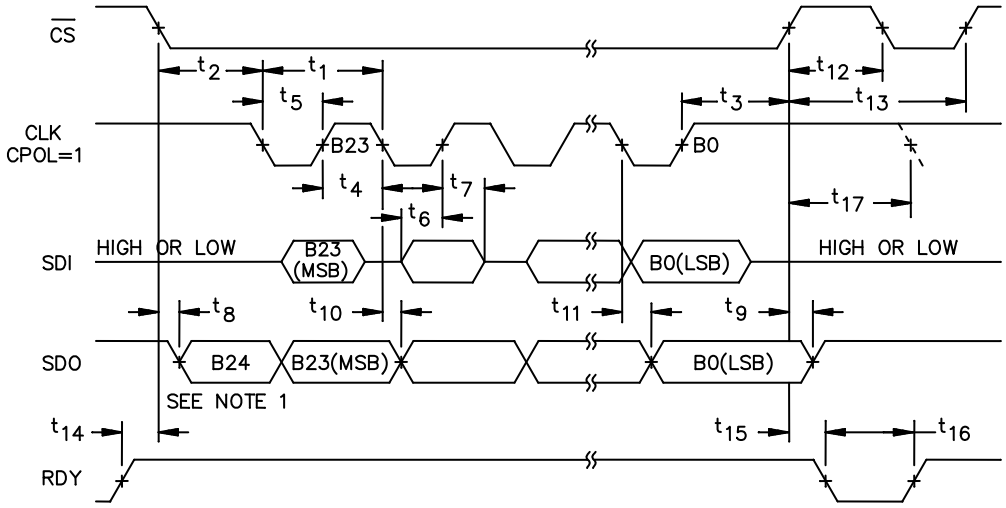


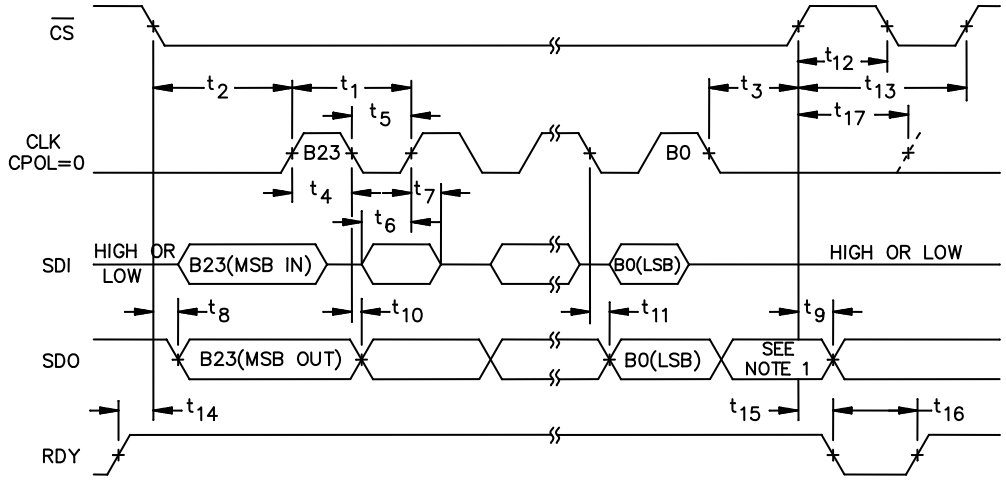
FIGURE 3. Functional block diagram.



CPHA=1

NOTES:
1. The extra bit that is not defined is normally the LSB of the character previously transmitted.
   The CPOL = 1 microcontroller command aligns the incoming data to the positive edge of the clock.

FIGURE 4. Timing diagram.



CPHA=0

NOTES:
1. The extra bit that is not defined is normally the MSB of the character just received.
   The CPOL = 0 microcontroller command aligns the incoming data to the positive edge of the clock.

FIGURE 5. Timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/11605-01XB	24355	AD5235BRU25-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605